

## Intel<sup>®</sup> ITANIUM™

For years, processor performance has obeyed the durable dictum of Moore's Law, started by Intel founder Dr. Gordon Moore. Now as business enters the 21<sup>st</sup> century, that law faces a challenge. The incredible growth in network traffic, coupled with sophisticated applications and rich data types, is placing unforeseen strains on servers, clients and workstations.



*The result: Demand for performance outstrips processor performance increases.*

**Foreseeing the Future:** The fact is, no one could have predicted ten years ago the impact that the Internet, e-business, and advanced collaborative technologies would be having on us today. E-commerce servers churn out millions of secure transactions every minute of everyday, while database servers manage dynamic, terabyte-sized stores of mission-critical information. Engineers and designers use workstations to develop complex models to physical product that can grow to hundreds of megabytes or even more in size.

In past, companies turned to proprietary processors based on Reduced Instruction Set Computing (RISC) to handle difficult workstation and server applications.

With the Itanium processor, Intel introduces Explicitly Parallel Instruction set Computing - known as EPIC - which enables Intel Itanium processors to work on as many as 20 operations at once.

The project **Merced / IA 64** is now christened as **Itanium**. The Itanium processor uses Explicitly Parallel Computing technology to enable breakthrough levels of performance in targeted application segments. EPIC's explicit parallelism provides the capability to execute multiple instructions simultaneously. EPIC also delivers new features such as predication and speculation to overcome legacy performance limitations such as instruction branches and memory latency.

The Itanium processor family extends open-standards-based computing to the enterprise and brings flexibility, choice and value over proprietary solutions. A broad range of Itanium-based software offerings from industry-leading vendors combined with IA-32 instruction binary compatibility in hardware providing an increased level of investment protection.

### Product Highlights

- Explicitly Parallel Instruction Computing (EPIC) technology enables up to 20 operations/clock.
- Three levels of cache reduce memory latency: 2MB / 4MB Level 3 cache, 96K Level 2 cache, and 32K Level 1 cache.
- Operating frequencies of 733MHz and 800MHz.
- 266MHz data bus enables fast system bus transactions with 2.1 GB/sec bandwidth.
- Advanced error detection, correction and containment provided by Machine Check Architecture (MCA), comprehensive error logging, and Error Correcting Code on caches and the system bus.
- System management features such as a thermal sensing device.
- IA-32 instruction binary compatibility in hardware.

### Performance

- Unified 2MB or 4MB on-cartridge L3 cache runs at full processor frequency and is organized as 4-way set-associative with 64-byte cache line size. Fully pipelined and optimized to provide fast access to data at a bandwidth of 12.8GB/sec using a 128-bit wide cache bus.

- Unified L2 cache is 96KB, 6-way set-associative, and fully pipelined with 64-byte cache line size.
- L1 cache, with separate instruction and data caches, is 32KB (16KB data / 16KB instruction), 4-way set-associative, and fully pipelined with 32-byte cache line size.
- Highly parallel, pipelined hardware with 10-stage pipeline. Floating-point (FP) unit containing two FMAC (Floating-Point Multiply Accumulate) units operates on 82-bit operands. Each FMAC unit can execute two floating-point operations per clock with single, double and double-extended precision.
- Two additional FP multimedia units are capable of executing two single-precision FP operations each. Combined with the regular FMACs, a total of eight single precision FP operations can be executed every cycle resulting in 6.4 GFLOPS maximum.

- Integrated system management features provide temperature monitoring and cartridge identification information.

**ITANIUM™ Architecture** Explicitly Parallel Instruction Set Computing (EPIC) technology increases Instruction Level Parallelism (ILP) by maximizing hardware-software synergy. The Itanium architecture provides mechanisms such as branch and cache hints for the compiler to communicate compiler time information to the processor.

In addition, the architecture allows compiled code to manage the processor hardware more efficiently through an innovative instruction format. These communication mechanisms minimize the cost of branches and reduce cache misses while enabling more parallelism.

- *Speculation:* Improves performance by allowing the compiler to schedule load instructions ahead of branches and stores to reduce memory latency.

- **Predication:** Improves performance by eliminating branches and associated branch misprediction penalties.

- **Parallelism:** Delivers higher performance and scalability by enabling the compiler to provide more information to the processor allowing it to execute multiple operations simultaneously on a sustained basis.

- **Register Stacking:** Reduces call/return procedure overhead via the flexible integer registers model managed by the Register Stack Engine (RSE).

- **Register Rotation:** Automatically renames registers in hardware to improve software loop performance without the additional overhead required in traditional methods.

- **SIMD Instructions:** Significantly improves Multimedia application performance by operating on multiple integer or floating-point operands per single instruction.

- **Branch/Memory Hints:** Improves branch prediction rate and reduces memory latency.

This architecture has massive register resources: 128 integer registers, 128 floating point registers, 8 branch registers, and 64 predicate registers.

### System Bus Architecture

- Increased bus efficiency through enhanced deferred transactions.
- 266MHz data bus (bus fraction 2:11 and 2:12).
- System data bus throughput up to 2.1GB/sec.
- 64-bit wide data bus (plus 8 bits of ECC).

### Availability

- Error Checking & Correction (ECC) provides increased availability, enabling detection and correction of data errors in L2 data cache, L3 tag and data cache, and processor data bus.

- Parity checking on L1 cache provides increased reliability by enabling detection of errors.

- Server Management features provide for increased system availability.

- \* Processor information ROM includes key processor information and built-in programmable EEPROM for special-purpose software (e.g., inventory management).

- \* Thermal sensor provides increased thermal management.

- Enhanced Machine Check Architecture enables processor, firmware and OS to cooperate to contain and fix errors, reducing downtime.

- Notification of corrected errors allows the OS/platform to maintain error statistics allowing proactive preventative actions and system maintenance decisions to be made.

- Processor watchdog timer detects system hang conditions.

### Scalability

- Scalability features enable large systems to scale to 32 processors and beyond with increased throughput.

### Link to the Present

Of course, most businesses can't afford to scrap one architecture for another - no matter the performance advantage, however, Itanium architecture offers full compatibility with the universe of existing applications and business systems written for the IA-32 processor family. An Itanium processor based workstation, for example, will seamlessly run existing e-mail, web browsing, and office productivity applications alongside advanced workstation software tuned for Intel Itanium architecture.

Operating systems like Microsoft Whistler (Win64), RedHat Linux 64, HP UX 11i V1.5 and AIX 5L are designed to use the maximum power of Itanium.

### So, where we go...

Ten years ago, no one would have guessed how the Internet would have transformed the business and computing landscape....

Then again, ten years ago no one would have anticipated solutions as powerful as these architectures too.....



**HCL**