Processor Packages

A raw processor chip is very small and fragile, and for this reason it is extremely difficult to make connections to it and easy to damage it. Chips are not placed into motherboards in their raw form, but rather after having been packaged in a material that protects them, allows them to dissipate heat properly, and has connectors of a standard size and shape. This allows motherboards to be made in a more standardized fashion without having to worry about the internal physical structure of the chip.

The structure of the packaging is linked inextricably to the socket or slot that the processor uses to interface to the motherboard. The package represents a way of connecting the microprocessor to the motherboard. The package assists in a space transformation in a controlled and economically viable manner.

Microprocessor packaging is undergoing major changes driven by technical, business, and economic factors. From the traditional role of a protective mechanical enclosure, the modern microprocessor package has been transformed into a sophisticated thermal and electrical management platform. Furthermore, microprocessor architecture and design techniques can have significant impact on the complexity and cost of packaging.

The key to packaging is to ensure that it enables and optimizes microprocessor performance. In its early evolution, the influence of the package on microprocessor performance was limited; however, as the microprocessor evolves to provide increasing

performance, the package must evolve to keep up, and packaging design must ensure that it optimally enables the microprocessor.

THE EVOLUTION OF PACKAGING

In the Beginning: The Mechanical Enclosure

For many years, wirebonding and ceramic packages were the base assembly technologies or microprocessors because of their versatility and reliability.

The first developed processors, used on the original PC, XT and clones, used standard ***Dual Inline or*** **DIP Packaging.**

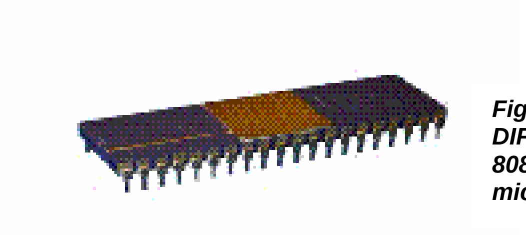


Figure 1 :
DIP package for 8086/88 microprocessors

”Dual inline” refers to two parallel sets of pins. DIP packaging is in fact the standard packaging used for most regular integrated circuits. Intel’s 4004 microprocessor and later, the 8080, 8086, and 8088 microprocessors were all housed in ceramic dual-in-line packages, that used wirebond connections. These microprocessors had new I/O pins (less than 40) and delivered very modest performance (<20Mhz). The primary function of the package was to provide space transformation of the I/Os in order to ease board routing and protect the chip from mechanical damage and from the environment. These were simple, single-layer packages.

Pin-Grid Array and Variations (PGA/SPGA/CPGA/PPGA)

In the i286 and i386 microprocessor generations, the number of I/O pins increased as greater functionality was incorporated into the microprocessor. This necessitated the use of Pin-Grid Array (PGA) packages in which a larger number of I/O connections could be accommodated in a

small area. Also, in the i386 generation, it became evident that the increasing clock frequencies and simultaneous I/O switching could cause unwanted noise problems. Consequently, design and modeling competencies were substantially enhanced to account for these factors leading to the first use of multilayer ceramic packages.

The Pin Grid Array Package is usually a square ceramic multilayer package with an array of “pins” brazed onto either the front side of the package (cavity down) or on the backside of the package (cavity up).

PGA packaging is the standard used for most of the processors, starting with the Intel 80286 over a decade ago. PGA packages are square or rectangular and have two or more rows of pins going around their perimeter. They are inserted into a special socket on the motherboard or daughtercard (Socket 1/2/…….7/8).

PGA comes in two different main material types. The standard PGA used on most processors until recently is made from a ceramic material, and is also called CPGA for that reason. Some newer processors use a plastic package, called PPGA. This plastic package is both less expensive and thermally superior to the CPGA. It has a raised metal square area on its surface for heat transfer to the heat sink that works better than the CPGA does.

Advantages of CPGA are:

- The ability to handle many I/O’s
- Rugged construction
- True hermetic encapsulation
- Small foot print relative to pin count
- Ease of PC board mounting via direct solder or using a socket.

In addition to the basic function of connecting the I/Os, advanced electrical design concepts were incorporated. These included the use of power and ground planes as well as the inclusion of integrated capacitors in the package. These features transformed the package from a simple mechanical enclosure to a mulilayer electrical distribution and signal-routing management platform.

The next-generation microarchitecture, commonly referred to as the P6 microarchitecture, called for a dedicated cache chip connected to the microprocessor via a Backside Bus (BSB). The first implementation of this architecture was on the Intel Pentium Pro Processor where the microprocessor and the cache chips were housed in a dual-cavity ceramic PGA package and connected by wire bonding.

The second-generation implementation of the same microarchitecture utilized a cartridge form-factor. In this instance, the microprocessor and cache chips were housed in separate component packages and were connected using a standard printed circuit board.

S.E.C.C (Single Edge Contact Cartridge) packaging:

To maintain a high-speed connection between the cache and the actual processor, the L2 cache was integrated with the processor package.

Using this technology, the core and L2 cache are fully enclosed in a plastic and metal cartridge. These sub-components are surface mounted directly to a substrate inside the cartridge to enable high frequency operation. The S.E.C cartridge technology allows the use of widely available, high-performance industry Burst Static RAMs (BSRAMs) for the dedicated L2 cache, enabling high-performance processing.

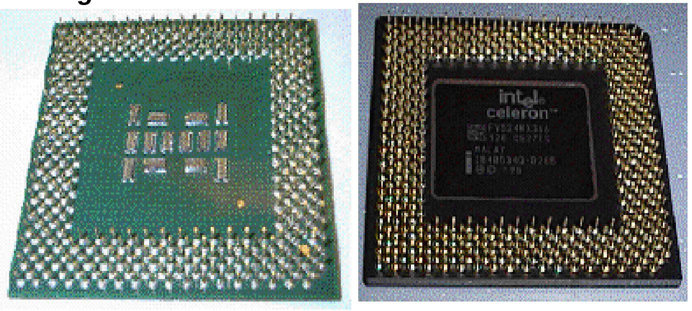
The Pentium II processor connects to a motherboard via a single edge connector instead of the multiple pins used in existing PGA packages. Similarly, the slot 1 connector replaces the PGA socket used in prior systems.

Flip Chip Pin Grid Array (FC-PGA) :

Silicon feature scaling and the integration of the Level 2 (L2) cache directly into the microprocessor die were key enablers to lower the cost of packaging. Without the need or the multidie package or cartridge to service the high-speed BSB, it was possible to move back to single-chip packaging. One of them is pinned packages for sockets in desktops; the package substrate is referred to as the Flip-Chip PGA substrate, another version of the organic substrate technology.

FC-PGA packages use chips that have been turned upside down and attached to the package or the board using solder balls instead of perimeter bonding wires. The solder balls are jointed directly to a set of solder balls on the substrate (the base layer of the chip and the electrical ground for the circuit). The exposed core rests on the actual package, and the chips make direct contact with the heat sink. This allows or more efficient cooling to take place. Since the chips are placed directly on the board, FC-PGA packages have a high I/O density and shorter electrical connections than other types of packaging. I/O’s can be from 2 to as much as 1700.

Figure 2: Underside Views of FC-PGA and PPGA Packages



PPGA **FC-PGA**

The Intel Celeron processor is packaged in a Flip Chip Pin Grid Array or Plastic Pin Grid Array package which includes the processor core and the connection pins. Figure 2 shows the 370 pins on the bottom of the processor package that provide the electrical connection via the 370-pin socket from the processor to the motherboard. Compared with the high-lead-count wire-bonded packages, flip-chip offers improved signal integrity to processors, SRAMs, chipsets and other cost-sensitive ICs.

The FCPGA package not only delivered a package with high performance on a cost-effective substrate, but also intelligently reused existing assembly equipment to minimize overall packaging cost. The need for high-density interconnects in a cost-effective flip-chip package was the motivation for FCPGA technology development. Flip-chips are found in consumer products like watches, smart cards,etc and in high end products like mainframe computers.

Conclusion

Package performance implies a clear understanding and optimization of the package’s thermal, electrical and mechanical characteristics to enable overall performance, power dissipation and to ensure mechanical robustness.

Recent advances in microprocessor packaging indicate a migration from wirebond to flip-chip; and from ceramic to organic packages, with multichip technologies emerging as key form factors.