

Sun System Architecture - 2

Sun Fireplane Interconnect is a high-speed system interconnect between the CPU, memory, and I/O subsystems in UltraSPARC III systems. The Sun Fireplane interconnect provides superior memory and I/O bandwidth, enabling the UltraSPARC III to deliver superior performance.

This is one of the industry's high-speed, redundant, reconfigurable crossbar system interconnect. It is reconfigurable because the system can start with a single crossbar segment to provide higher performance, then switch to two crossbar segments when the business demands more isolation and protection of the domains.

It is redundant because any domain affected by a failed segment can be brought up on the surviving segment.

In the design of the Sun Fire 6800, this redundancy enables Sun to offer the first cluster in a box with no single point of failure that would affect both segments. The Sun Fireplane interconnect can also perform the following functions:

- ✍ Divide the system into completely isolated segments
- ✍ Divide segments into logically isolated domains
- ✍ Hot-plug and unplug individual boards

Key Features of the Sun Fireplane interconnect include the following:

- ✍ 150-MHz operating frequency for increased performance over previous designs.

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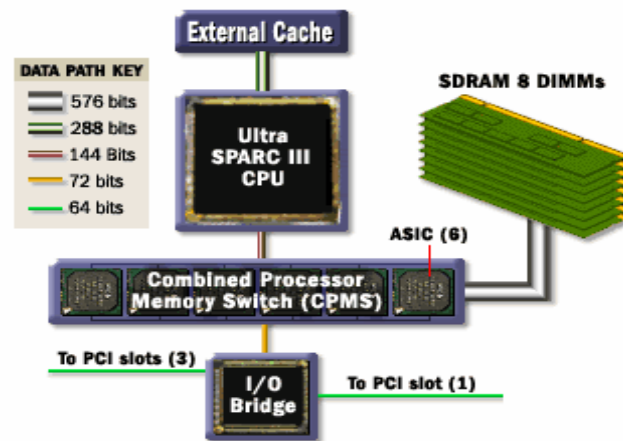
- ✍ Total throughput of up to 9.6 Gbyte / sec (two-processor system)
- ✍ Low-latency memory access
- ✍ Out-of-order transaction processing enables multiple "in-flight" transactions on the bus at one time
- ✍ Separate address/control and data paths for flexible implementation
- ✍ High-throughput paths to memory clocked at 150 MHz (576-bit wide paths including ECC)
- ✍ Integrated support for multiprocessor configurations

Key Benefits:

The key benefits of the Sun Fireplane interconnect include:

- ✍ **High bandwidth** - The Sun Fireplane interconnect takes advantage of very large scale integration (VLSI) and packaging technology improvements by widening the data path segments to 288 bits.

With a 150-MHz clocking rate, the interconnect delivers 9.6 Gbytes per second of sustainable bandwidth. The use of segments delivers higher



availability but lower bandwidth per segment.

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- ✍ **Low latency** - Integrating the memory controller with the CPU reduces latency by up to 20% in single-processor systems (10% in dual-processor systems) without software optimization. The Sun Fireplane interconnect also minimizes latency by implementing special techniques for delivering data to the caches, and the UltraSPARC III provides a sophisticated write-buffer with headroom so that even worst - case circumstances do not impact performance.
- ✍ **Innovative flow control** - During write transactions, the Sun Fireplane interconnect enables the target device to pull data rather than it being pushed by the writer, as in previous-generation systems. This approach enables a balanced usage of system bandwidth between processors and translates into a more predictable response time under heavy load.

New signaling technology - The Sun Fireplane interconnect introduces a low-level voltage signaling technology called dynamic transceiver logic (DTL). DTL provides circuitry that compensates automatically for voltage, temperature, and process variations in chips, translating into higher clock frequency on wide data paths.

How it Works: The diagram (page 2) illustrates the architecture with the UltraSPARC III processor and Sun Fireplane interconnect data path. The interconnect data path is a 288-bit on-chip bus implemented inside a set of six identical ASICs (application-specific integrated circuits). This structure couples a wide data path with a high clock frequency of 150 MHz. The connection between the Sun Fireplane interconnect devices (UltraSPARC III and a

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custom I/O bridge) and the data path ASICs uses a point-to-point model that enables the best possible clocking rate for chip-to-chip communication.

The data path ASICs, called the combined processor memory switch, also provide a switch between the internal data bus and the responding interconnect device (UltraSPARC III and custom I/O bridge).

With the bus model of the Sun Fireplane interconnect, the need for a centralized system controller is eliminated, and control is distributed between all attached devices. The arbitration for the address and control lines is performed simultaneously by all devices, which has the added benefit of reducing latency.

Memory Subsystem:

In the UltraSPARC III / Sun Fireplane interconnect system architecture, the UltraSPARC III performs the memory controller function through its external memory unit (EMU), rather than a centralized memory controller (located in the system controller on UltraSPARC II / UPA systems). The memory controller function is shared by all Sun Fireplane interconnect devices in the system.

☞ **External cache memory** - UltraSPARC III feature 4 or 8 MB of external secondary cache. Synchronous SRAMS are used for data and for tag. The data path to the external cache is 288 bits wide and is parity protected.

☞ **Main memory** - The data path to the main memory (DIMMs) is 576 bits wide, increasing memory system performance.

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Cache Coherency:

UltraSPARC III external cache is located on the processor module. Data that has been recently used, or whose impending use is anticipated, is retrieved and kept in cache memory - closer to the processor that will need it. In a multiprocessor, shared-memory system, the task of keeping all of the different caches within the system consistent requires assistance from the system interconnect.

The Sun Fireplane interconnect implements cache coherency through a technique known as snooping. With this approach, each cache monitors the addresses of all transactions on the system interconnect, watching for transactions that update addresses it already possesses. Since all processors need to see all of the addresses on the system interconnect, UltraSPARC III systems connect the address and command lines to both UltraSPARC III processors to eliminate the need for a central controller.

Gigaplane Bus

Enterprise X500 servers implement a centerplane architecture called the Gigaplane system bus. The Gigaplane bus is the central path that links the CPU and memory to peripherals that enter through I/O cards. Developed for simplicity, high capacity, and reliability, the Gigaplane bus substantially improves raw system bus and I/O performance.

The packet-switched design uses separate buses for address and data, resulting in high utilization of the potential peak bandwidth and reducing latency. This design provides a faster transfer rate than system buses that share a single path for address and data.

Key Benefits

Low Latency: The low-latency, packet-switched Gigaplane bus uses separate paths for address, data, and control lines, resulting in extremely high use of the

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potential peak bandwidth. Maximum throughput is 2.68 Gbyte / sec at 84 MHz and 3.2 Gbyte / sec at 100 MHz.

Scalability: The X500 server Gigaplane bus runs at optimal performance with processor speeds faster than 336 MHz. It runs at a maximum speed of 100 MHz with the 400 MHz processor, and will support future, faster processors.

The previous-generation X000 server Gigaplane bus runs at a maximum speed of 84 MHz-sufficient enough to support current UltraSPARC processors running up to 336 MHz.

Past three months, we have covered the Fundas of Sun Technologies like UltraSPARC Processors, SBus, VIS, UPA, Graphics subsystem, Sun Fireplane Interconnect and Gigaplane.

We shall be covering Solaris and Solutions in the months to come.

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